

SPECIFICATION FOR AMOLED Module

MODULE No:	ID-020HVOIN002-C002B
CUSTOMER:	

I DISPLAY	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

[illegible]

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* **Description**

This is a color active matrix AMOLED module using Low Temperature Poly-silicon Thin Film Transistors as active switching devices. This module has a 2.06 inch diagonally measured active area with 410 horizontal by 502 vertical pixel arrays. Each pixel is divided into RED and GREEN dots, or BLUE and GREEN dots, and two pixels share RED or BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors.

* **Features**

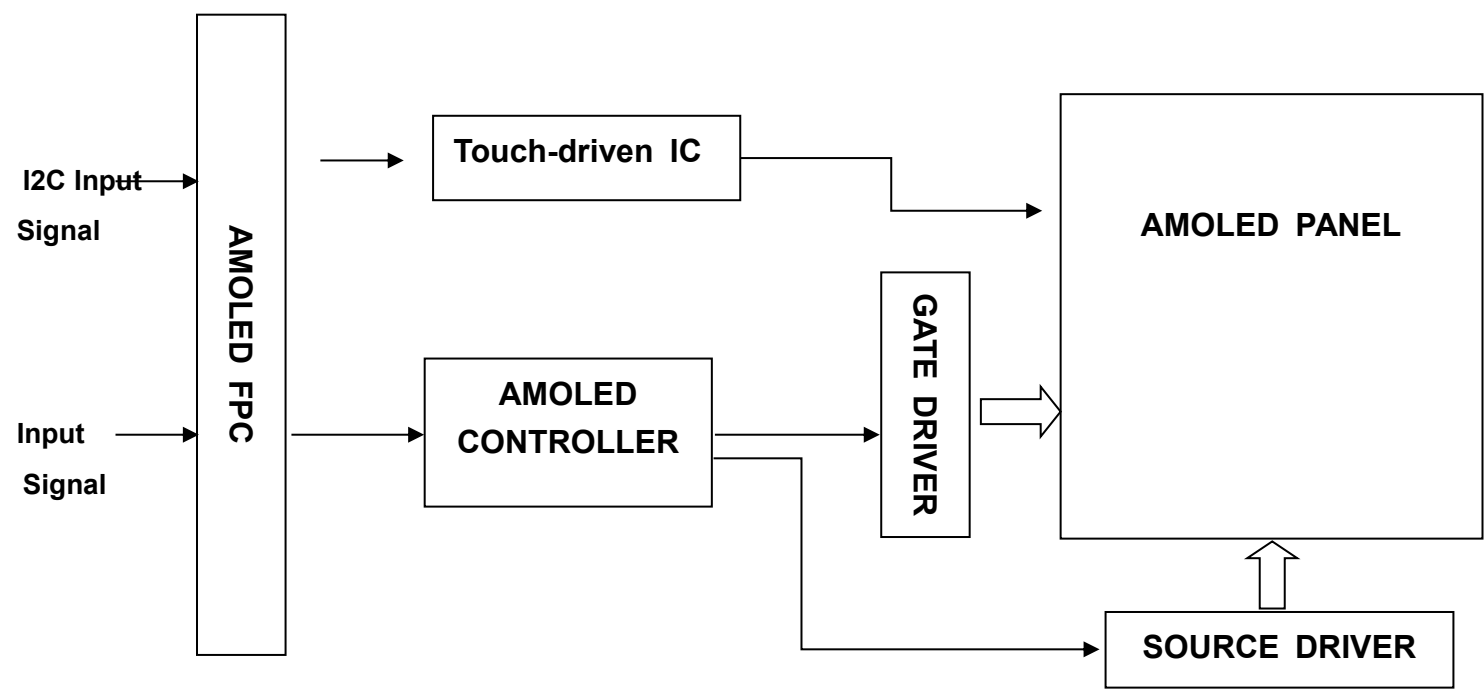
General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	33.09*40.51 (2.06 inch)	mm	
Display colors	16.7M	colors	
Pixel pitch	80.7(H)*80.7(V)	um	
Number of pixels	410(RGB)*502	dots	
Viewing angle	ALL	o'clock	
Controller IC	CO5300	-	
Touch Controller IC	CST916E(Oncell)	-	
LCM Interface	MIPI	-	
Display mode	AMOLED	-	
Operating temperature	-20~+60	℃	
Storage temperature	-30~+70	℃	

* **Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		37.35		mm	-
	Vertical(V)		45.15		mm	NOT2
	Depth(D)		2.31		mm	NOT1
Weight			8		g	-

NOT1: Flat thickness without any bending
NOT2: Including the length of the FPC after bending

1. Block Diagram



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3. Input terminal Pin Assignment

Connector: OK-14GM024-04

NO.	SYMBOL	DISCRIPTION	I/O
1	TP_GND	Ground	P
2	TP_VDD_3.3V	Power Supply for touch IC	P
3	TP_RST_3.3V	Touch Panel Reset	I
4	TP_INT _3.3V	Touch Panel Interrupt	P
5	GND	Ground	P
6	MDSI_DP0	Positive polarity of low voltage differential data 0 signal	I/O
7	MDSI_DN0	Negative polarity of low voltage differential data 0 signal	I/O
8	GND	Ground	P
9	MDSI_CP	Positive polarity of low voltage differential clock signal	I
10	MDSI_CN	Negative polarity of low voltage differential data 0 signal	I
11	GND	Ground	P
12	RESET (1.8V)	Reset signal pin , Active low.	I
13	FMARK (1.8V)	Output a frame head pulse signal	O
14	GND	Ground	P
15	IOVDD_1.8V	Power supply for digital system and booster circuit	P
16	VCI_EN_2.8V	Power IC for analog system and booster circuit	P
17	MTP	NC	-
18	NC	NC	-
19	VBAT	Power IC for analog system and booster circuit	P
20	VBAT	Power IC for analog system and booster circuit	P
21	GND	Ground	P
22	TP_SCL_3.3V	Touch Panel Clock	I
23	TP_SDA_3.3V	Touch Panel Data	I\O
24	TP_GND	Ground	P

4. AMOLED Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal	TBD	--	--		(1)(2)
LCM Luminance		LV	White Mode	--	550	--	cd/m2	
Color gamut		S(%)	vs. NTSC	90	100	--	%	(1)
Color Filter Chromaticity	White	W_X		-0.04	0.302	+0.04		(1)(4)
		W_Y			0.314			
	Red	R_X			0.672			
		R_Y			0.325			
	Green	G_X			0.225			
		G_Y			0.683			
	Blue	B_X			0.139			
		B_Y			0.045			
OLED Life Time				30000	--	--	Hrs	
Option View		ALL						

Measuring Condition

Measuring surrounding : dark room

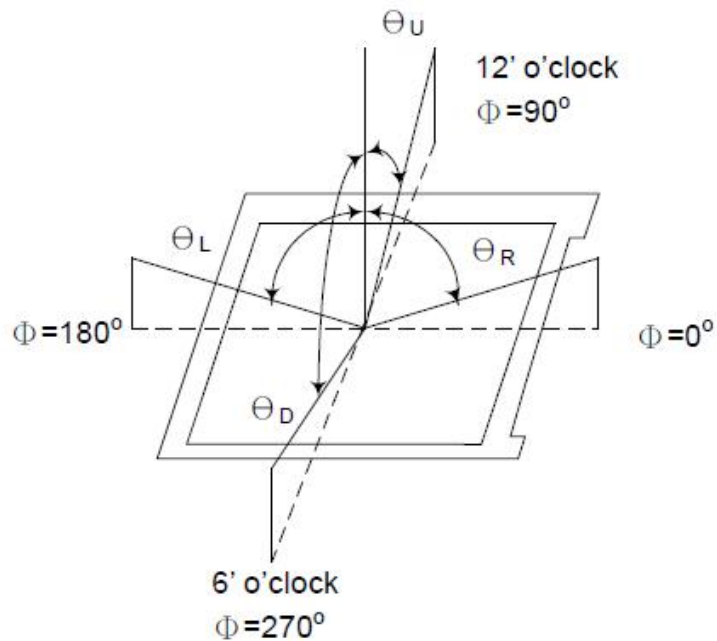
Ambient temperature : 25±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

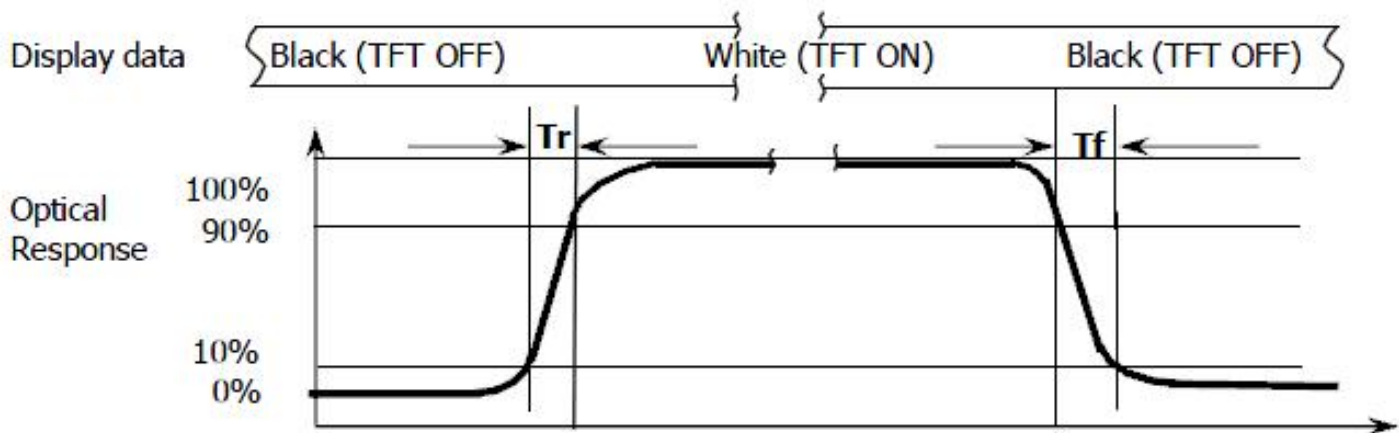
Note (1): Definition of Viewing Angle :



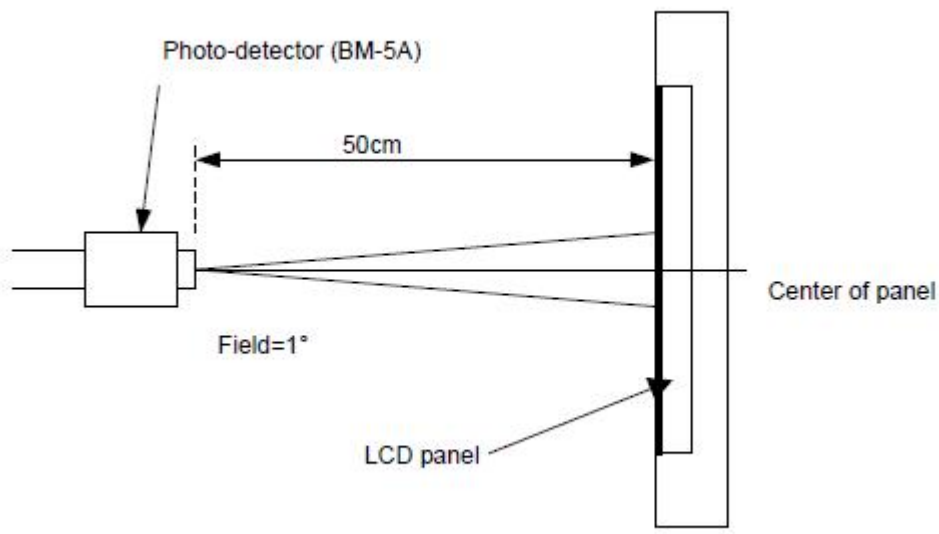
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. AMOLED Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit	Note
Power IC Supply	VBAT	-0.3	5	V	
Analog Power Supply Voltage	VCI_EN	-0.3	3.6	V	
I/O Power Supply Voltage	IOVDD	-0.3	3.3	V	
Operating temperature	T _{OP}	-20	+60	°C	
Storage temperature	T _{ST}	-30	+70	°C	

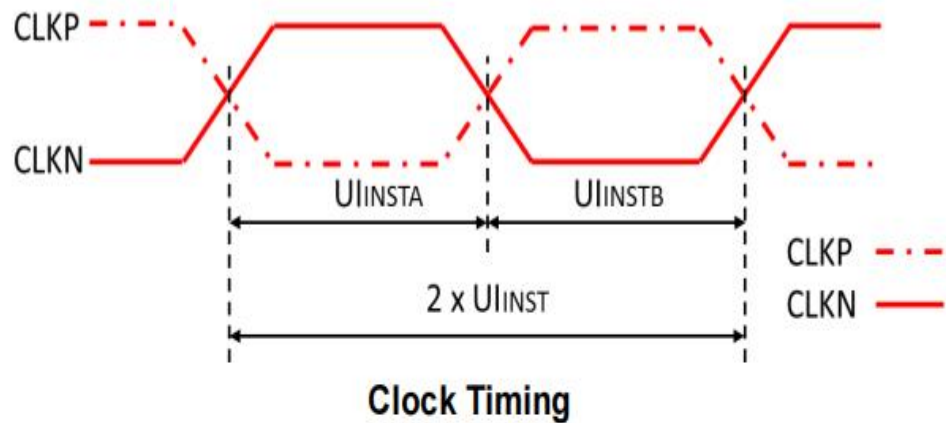
NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	VCI_EN	2.5	2.8	3.3	V	
I/O Supply Voltage	IOVDD	1.65	1.8	3.3	V	
Power Supply Voltage	VBAT	2.9	3.7	5	V	

6. AC Characteristic

6.1 High Speed Mode - Clock Timing

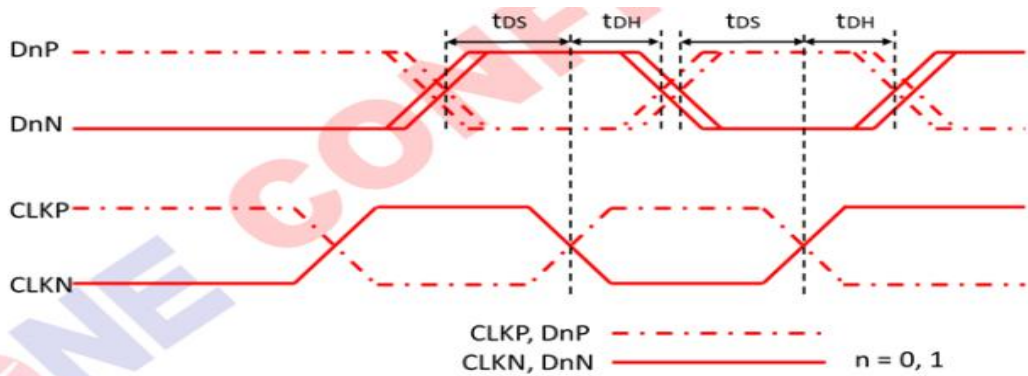


High Speed Mode - Clock Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	$2 \times UI_{INST}$	Double UI instantaneous	4		25	nS	
CLK P/N	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	2		12.5	nS	1

Note 1: $UI = UI_{INSTA} = UI_{INSTB}$.

6.2 High Speed Mode -Clock / Data Timings



DSI Clock / Data Timings

High Speed Mode - Clock / Data Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N (n=0, and1)	tDS	Data to Clock Setup time	$0.15 \times UI$			UI	
	tDH	Clock to Data Hold time	$0.15 \times UI$			UI	

6.3 High Speed Mode - Rising and Falling Timings

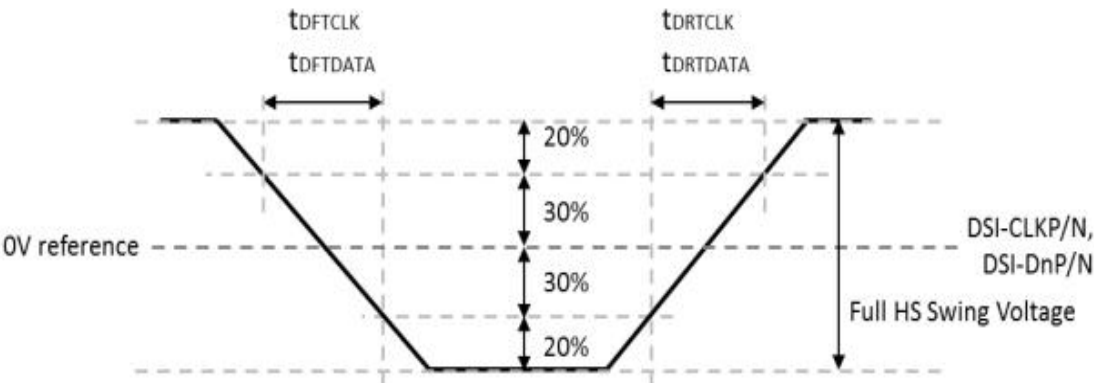


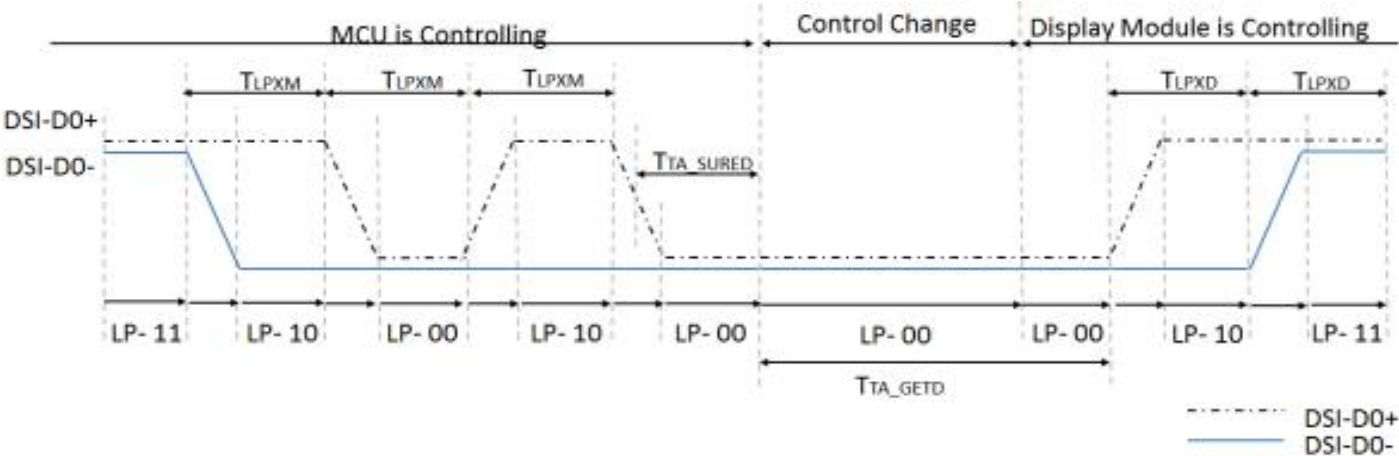
Figure 6-2 Rising and Falling Timings

High Speed Mode - Rising and Falling Timing

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150pS		$0.3 \cdot UI$		2,3
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N	150pS		$0.3 \cdot UI$		1,2,3
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150pS		$0.3 \cdot UI$		2,3
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N	150pS		$0.3 \cdot UI$		1,2,3

- Note 1:** DnP/N, n =0, and 1.
- Note 2:** The display module has to meet timing requirements, which are defined for the transmitter (MCU) on **MIPI D-PHY** standard.
- Note 3:** DSI-CLK+ = CLKP.
DSI-CLK- = CLKN.
DSI-D0+ = D0P.
DSI-D0- = D0N.

6.4 Low Speed Mode - Bus Turn Around



Bus Turnaround (BTA) from MCU to display module Timing

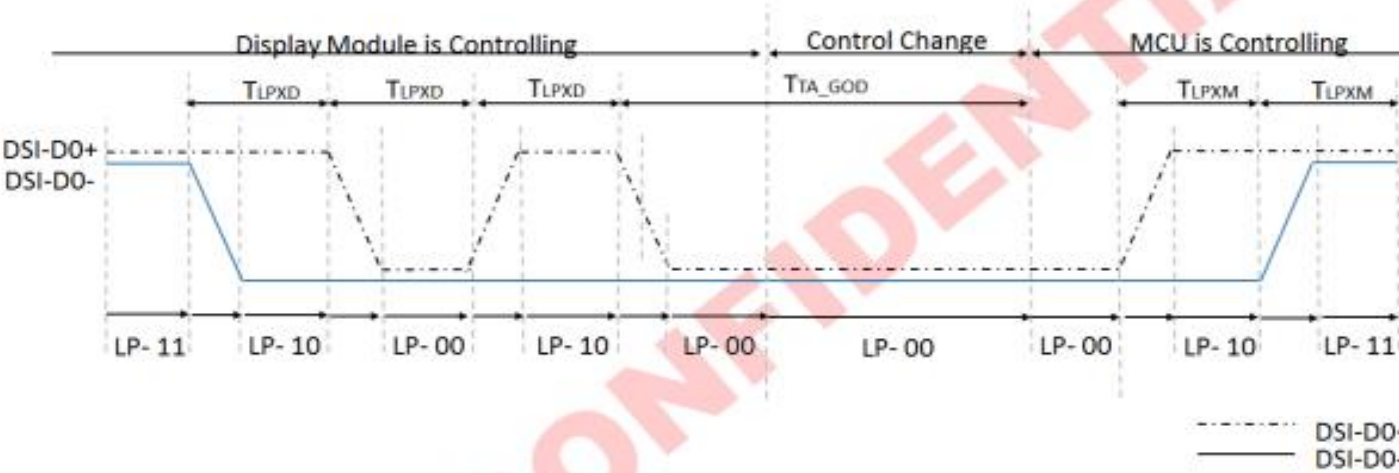


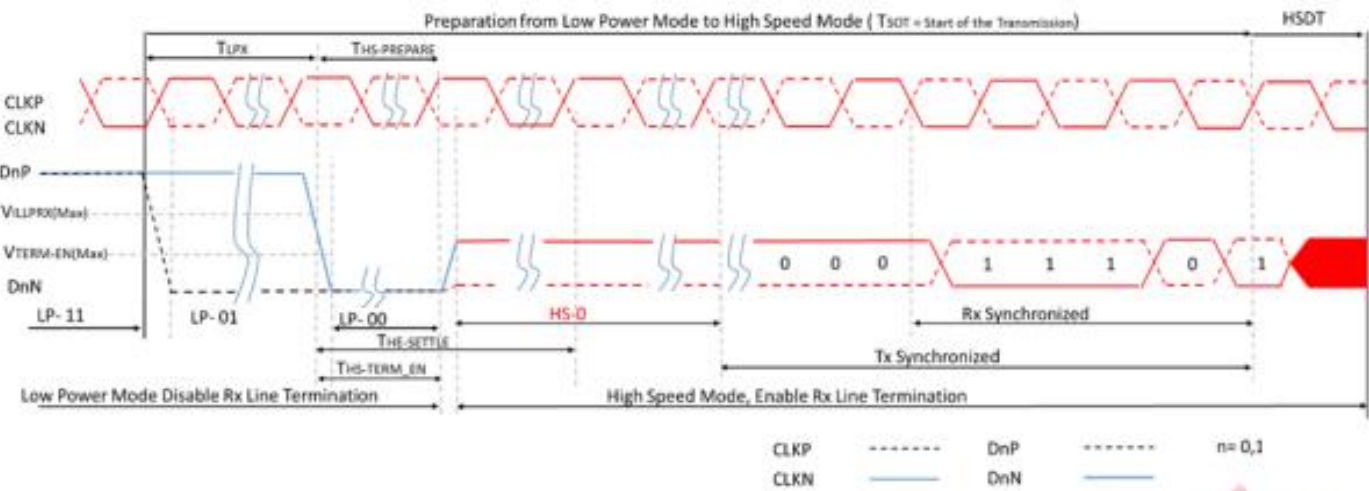
Figure 6-3 Bus Turnaround (BTA) from Display module to MCU Timing

Low Speed Mode - Bus Turn Around Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	TLPXM	Length of LP-00,LP-01,LP-10 or LP11 periods MCU to Display Module	50		75	nS	1
D0P/N	TLPXD	Length of LP-00,LP-01,LP-10 or LP11 periods Display Module to MCU	50		75	nS	1
D0P/N	TTA_SURED	Time-out before the Display Module starts driving	TLPXD		2* TLPXD	nS	1
D0P/N	TTA_GETD	Time to drive LP-00 by Display Module	5* TLPXD			nS	1
D0P/N	TTA_GOD	Time to drive LP-00 after turnaround request -MCU	4 * TLPXD			nS	1

Note 1: D0P = DSI-D0+, D0N = DSI-D0-.

6.5 Data Lanes from Low Power Mode to High Speed Mode



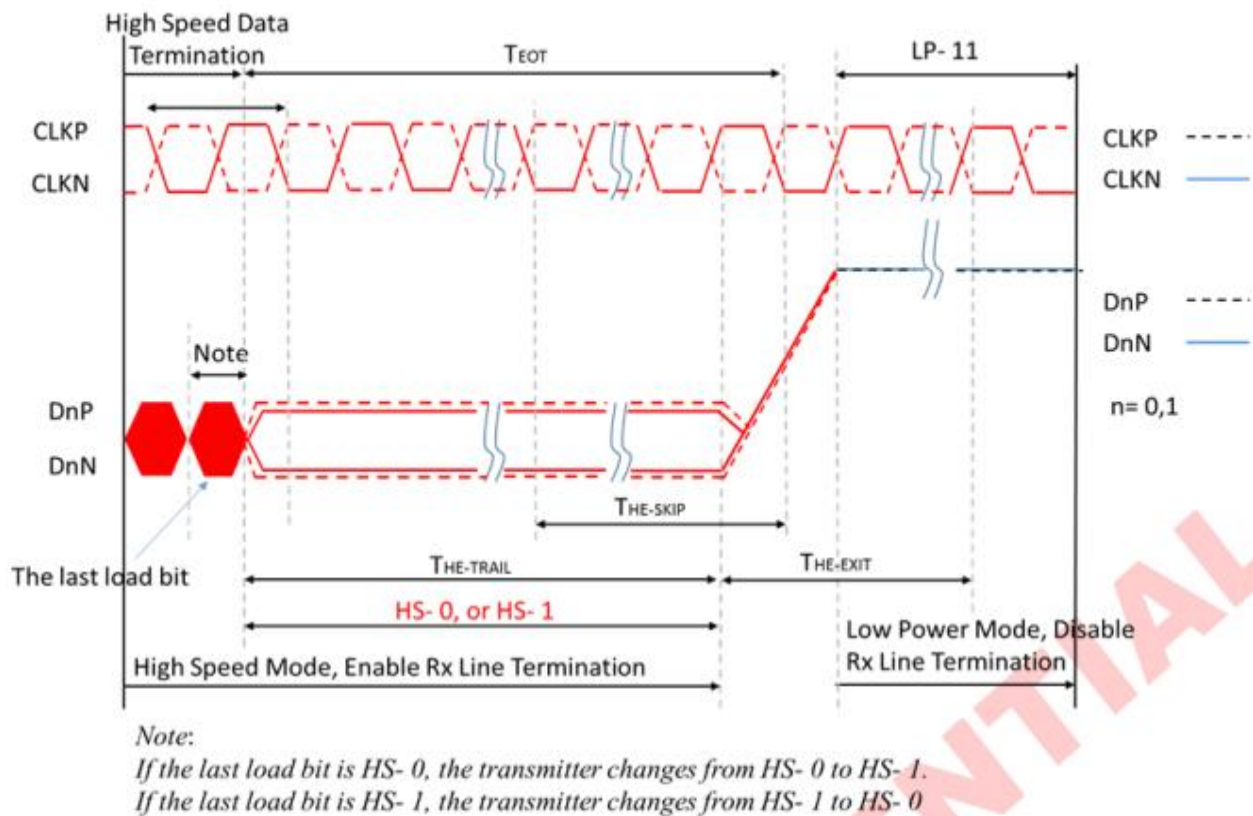
Data Lanes from High Speed Mode to Low Power Mode Timing

Data Lanes from Low Power Mode to High Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	T _{LPX}	Length of any Low Power State Period	50			nS	1
DnP/N	T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	T _{HS-TREM-EN}	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: DnP/N, n=0, and 1

6.6 Data Lanes from High Speed Mode to Low Power Mode



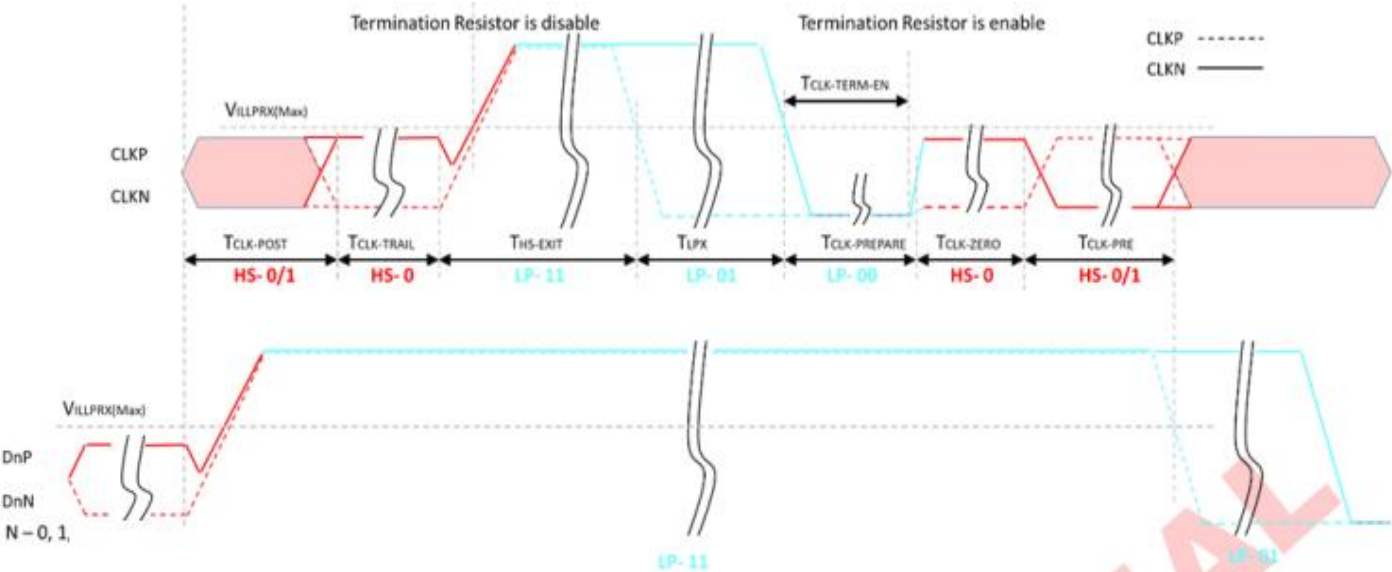
Data Lanes from High Speed Mode to Low Power Mode Timing

Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	T _{HS-SKIP}	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100			nS	1

Note 1: DnP/N, n=0, and 1.

6.7 DSI Clock Burst- High speed mode to /from Low Power Mode

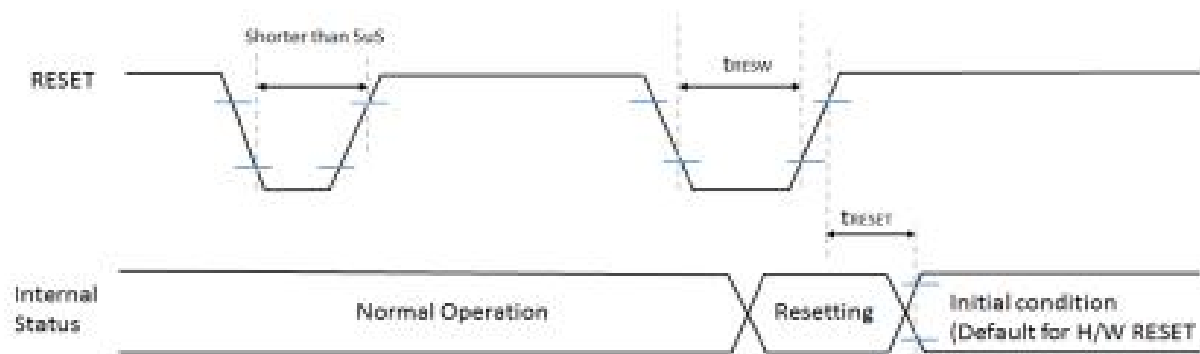


Clock Lane –High speed mode to / from Low Power Mode Timing

DSI Clock Burst – High speed mode to /from Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CKP/N	TCLK-POST	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CKP/N	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CKP/N	THS-EXIT	Time to drive LP-11 after HS burst	100			nS	
CKP/N	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CKP/N	TCLK-TERM-EN	Time-out at Clock Lane to enable HS termination			38	nS	
CKP/N	TCLK-PREPARE+TCLK-ZERO	Minimum lead HS-0 drive period before starting Clock	300			nS	
CKP/N	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

6.8 Reset input Timing



Reset Input Timing

Condition : Ta =25°C

Reset Input Timing

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	tRESW	Reset "L" pulse width		10			µS	1
	tRESET	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

Note 1: Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

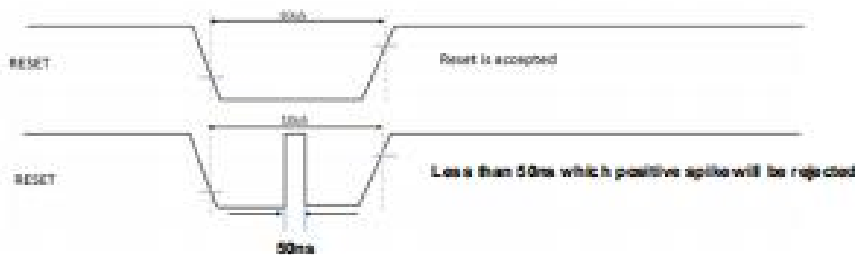
Reset Input Actions

RESET Pulse	Action
Short than 5µs	Reset Rejected
Long than 10µS	Reset
Between 5µs and 10µS	Reset Start

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for HW RESET.

Note3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is HW RESET complete time(tRESET) within 5ms after a rising edge of RESET.

Note4: Spike Rejection also applies during a valid reset pulse as shown below.



Note5: It is necessary to wait 5ms after releasing RESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. Quality Level

7.1 Standard

According to GB/T2828.1-2003/ISO 2859-1:1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II and based on Major Defect: AQL 0.65, Minor Defect: AQL 1.5.

7.2 Definition

- 1) Major Defect: The defect that greatly affect the usability of product.
- 2) Minor Defect: The other defects, such as cosmetic defects, etc.
- 3) Definition of Inspection Zone 检验区的定义:

Zone A: Active Area

Zone B: Viewing Area except Zone A Zone

C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

7.3 Inspection Methods

1. General Inspection: under 20W x 2 or 40W fluorescent light(1000+200LUX), about 30cm viewing distance, within 45° viewing angle, under 25±5℃.

Inspection Pattern: Red/Green/Blue/White/Black/128 gray scale

2. The Brightness and Color Coordinate Inspection: By CS2000/09A-OLED-117 or the equal equipment, in the dark room, under 25±5℃.

8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	60°C,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the OLED; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20°C, 96HR	
High Temperature Storage	70°C, 96HR	
Low Temperature Storage	-30°C, 96HR	
High Temperature & High Humidity Storage	+60°C, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-20°C,30 min ↔ 70°C,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±4KV, 5times; Contact:±4KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	

- Remark:
- 1.The test samples should be applied to only one test item.
 - 2.Sample size for each test item is 5~10pcs.
 - 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
 - 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
 - 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
 - 6. The color fading mura of polarizing filter should not care.

9. Cautions and Handling Precautions

9.1 Handling Precautions:

- (1) The display panel is made of glass and polarizer. As glass is fragile. It tends to become chipped during handling especially on the edges. Please avoid dropping or jarring. Do not subject it to a mechanical shock by dropping it or impact.
- (2) Do not apply excessive force to the display surface or the adjoining areas since this may cause abnormal. Do not touch the display with bare hands. This will stain the display area (some cosmetics are determined to the polarizer).
- (3) The polarizer covering the display surface of the OLED module is soft and easily scratched. Handle this polarizer carefully. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.). Do not put or attach anything on the display area to avoid leaving marks on it. Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizer. After products are tested at low temperature they must be warmed up in a container before coming in to contact with room temperature air.
- (4) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents.
- Isopropyl alcohol
 - Ethyl alcohol
- Do not scrub hard to avoid damaging the display surface.
- (5) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.
- Water
 - Ketone
 - Aromatic solvents
- Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading. Avoid contact with oil and fats.
- (6) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
- (7) When mounting the OLED module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable.
- (8) Do not attempt to disassemble or process the OLED module.
- (9) NC terminal should be open. Do not connect anything.
- (10) If the logic circuit power is off, do not apply the input signals.
- (11) To protect the display surface, the AMOLED Module is coated with a film. Be careful when peeling off this protective film, because static electricity may generate.

10. Packing

----TBD-----