

SPECIFICATION FOR AMOLED Module

MODULE No:	ID-027WVOIN011
CUSTOMER:	

I-DISPLAY	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

[illegible]

Part. No	ID-027WVOIN011	REV	V1.1	Page 2 of 31
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Contents

1. Block Diagram	5
2. Outline dimension	6
3. Input terminal Pin Assignment	7
3.1 OLED PIN	7
4.1 Optical specification	9
5. AMOLED Electrical Characteristics	12
5.1 Absolute Maximum Rating (Ta=25 VSS=0V)	12
5.2 DC Electrical Characteristics	13
6. AC Characteristics	14
6.1 Serial Interface Characteristics	14
6.2 RGB Interface Characteristics	15
6.3 DSI Timing Characteristics	16
6.4 Reset Timing	18
6.5 Touch Panel I2C Timing Characteristics	19
6.6 Touch Panel Reset Timing Characteristics	20
7. Recommended Operating Sequence	21
7.1 Display Power on/off Sequence	21
7.2 Touch Panel Power on Sequence	22
8. AMOLED Module Out-Going Quality Level	23
8.1 VISUAL & FUNCTION INSPECTION STANDARD	23
8.1.1 Inspection conditions	23
8.1.2 Definition	23
8.1.3 Sampling Plan	24
8.1.4 Criteria (Visual)	25
9. Reliability Test Result	29
10. Cautions and Handling Precautions	30
10.1 Handling Precautions:	30
10.2 Storage Precautions	30
10.3 Transportation Precautions:	30
11. Packing	31

* **Description**

This is a color active matrix AMOLED module using Low Temperature Poly-silicon Thin Film Transistors as active switching devices. This module has a 2.69 inch diagonally measured active area with 800 horizontal by 600 vertical pixel arrays. Each pixel is divided into RED and GREEN dots, or BLUE and GREEN dots, and two pixels share RED or BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors.

* **Features**

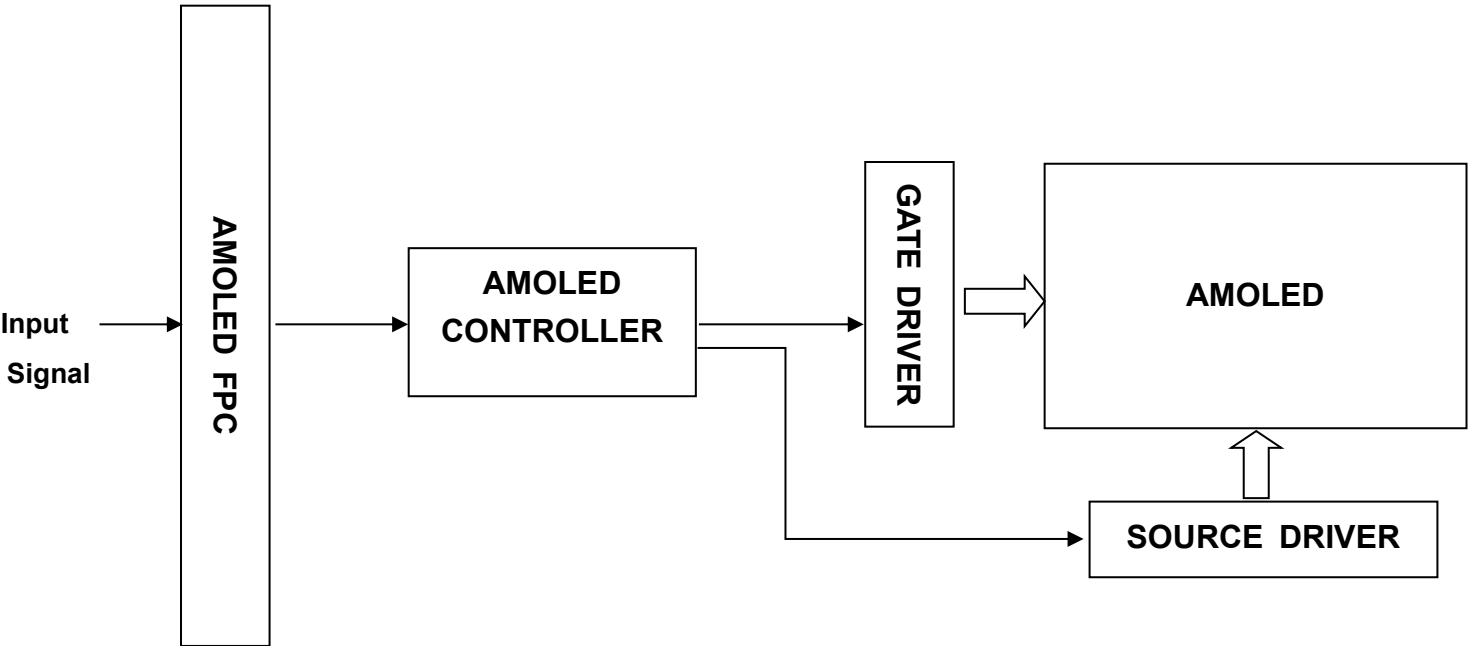
General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	54.6(H)*40.95(V) (2.69 inch)	mm	
Driver element	TFT active matrix	-	
Display colors	16.7M	colors	
Number of pixels	800(RGB)*600	dots	
Viewing angle	ALL	o'clock	
Controller IC	RM69700	-	
LCM Interface	MIPI	-	
Display mode	AMOLED	-	
Operating temperature	-40~+85	℃	
Storage temperature	-55~+125	℃	

* **Mechanical Information**

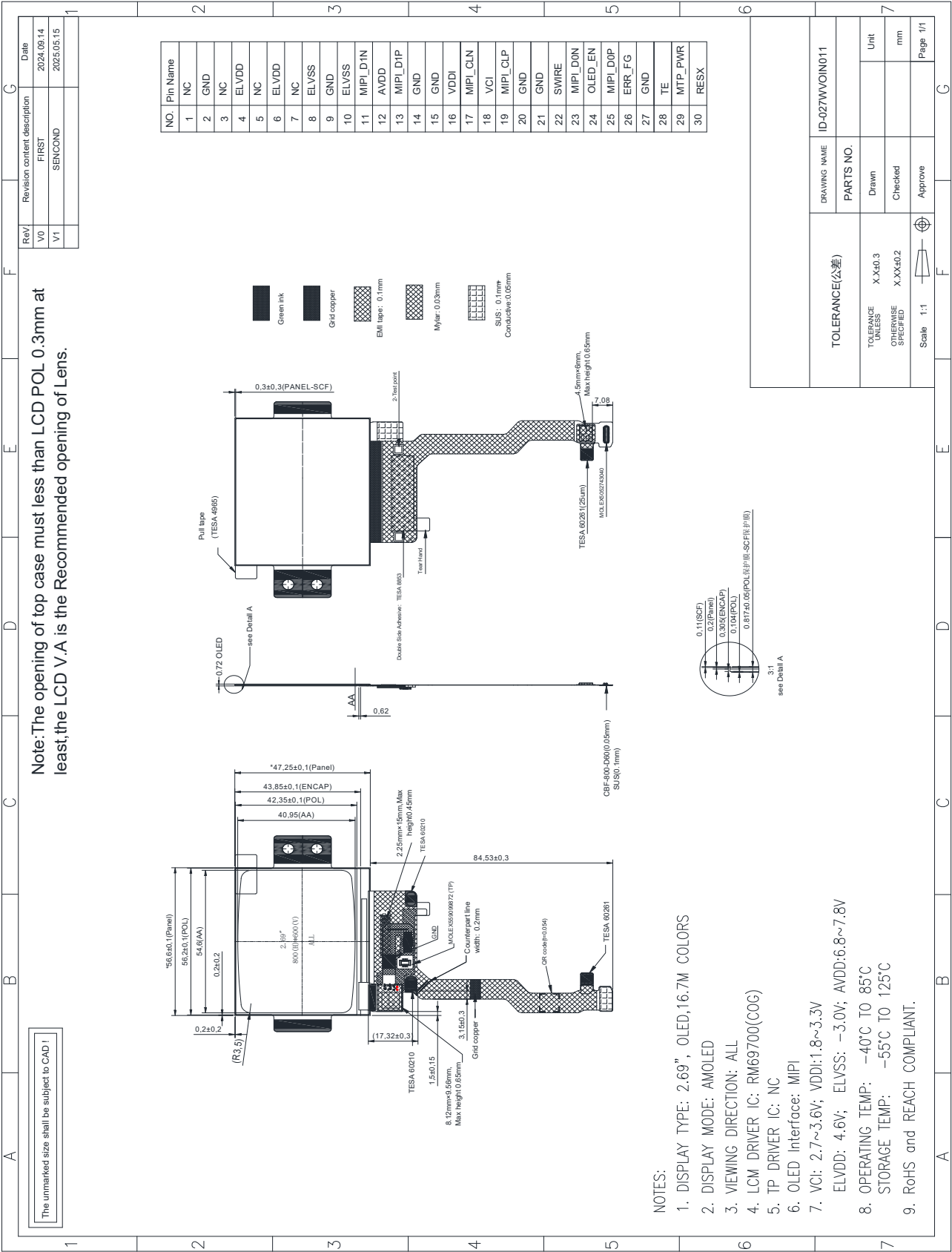
Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	--	56.6	--	mm	-
	Vertical(V)	--	47.25	--	mm	-
	Depth(D)	--	1.5	--	mm	-
Weight		--	4	--	g	-

Note: This product is equipped with a touch connector, but touch cannot be used due to the lack of complete IC register data.

1. Block Diagram



2. Outline dimension



TOLERANCE(公差)	DRAWING NAME		ID-027WV01011
	PARTS NO.		
TOLERANCE UNLESS OTHERWISE SPECIFIED	Drawn	Unit	
	Checked	mm	
Scale 1:1		Approve	Page 1/1

3. Input terminal Pin Assignment

3.1 OLED PIN

connector: Molex5052743040

NO.	SYMBOL	DISCRIPTION	I/O
1	NC	-	-
2	GND	Ground	P
3	NC	-	-
4	ELVDD	AMOLED power positive	P
5	NC	-	-
6	ELVDD	AMOLED power positive	P
7	NC	-	-
8	ELVSS	AMOLED power negative	P
9	GND	Ground	P
10	ELVSS	AMOLED power negative	P
11	D1N	MIPI Data Line	I
12	AVDD	AMOLED charge pumping power for DDIC	P
13	D1P	MIPI Data Line	I
14	GND	Ground	P
15	GND	Ground	P
16	VDDIO	AMOLED logic power for DDIC	P
17	CLKN	MIPI CLK Line	I
18	VCI	AMOLED logic power for DDIC	P
19	CLKP	MIPI CLK Line	
20	GND	Ground	P
21	GND	Ground	P
22	SWIRE	Control the PMIC	O
23	D0N	MIPI Data Line	

24	OLED_EN	OLED enable	
25	D0P	MIPI Data Line	
26	ERR_FG	NC	
27	GND	Ground	P
28	TE	Tear Effect	O
29	MTP_PWR	Power supply for MTP Programming or Erase (NC)	I
30	REST	Drive IC reset	I

4. AMOLED Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal	100000	--	--		(1)(2)
LCM Luminance		LV	White Mode	350	400	--	cd/m2	(6)
Color gamut		S(%)	vs. NTSC	--	100	--	%	(1)
Color Filter Chromaticity	White	W _X		-0.04	0.2985	+0.04		(1)(4)
		W _Y			0.3178			
	Red	R _X			0.6774			
		R _Y			0.3229			
	Green	G _X			0.2307			
		G _Y			0.6823			
	Blue	B _X			0.1395			
		B _Y			0.0504			
OLED Life Time			50%Bright ness drop @250cd/m 2,FullWhite	--	30000	--	Hrs	
Option View		ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

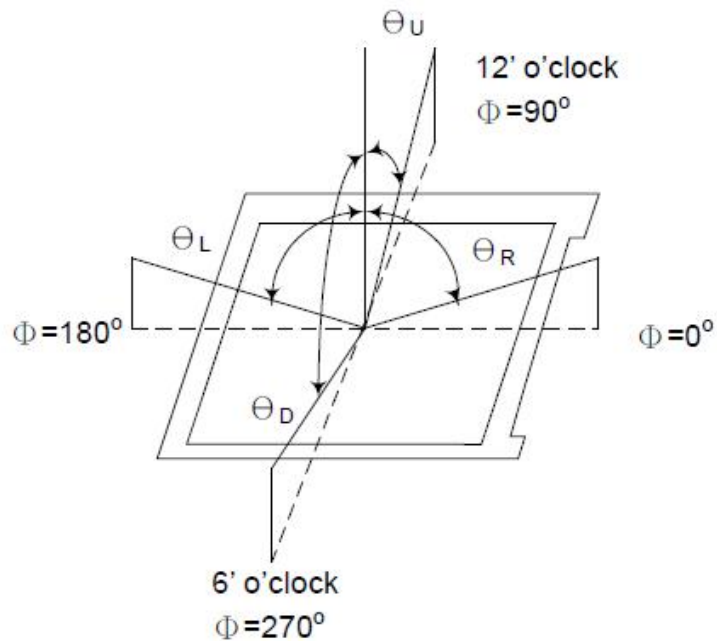
Ambient temperature : 25±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1): Definition of Viewing Angle :



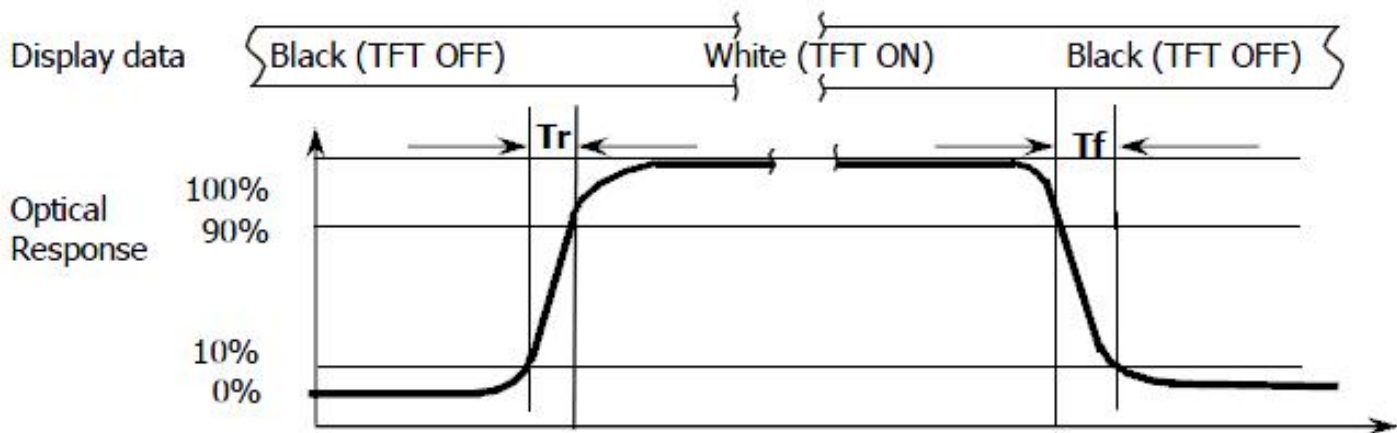
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

Luminance with all pixels white

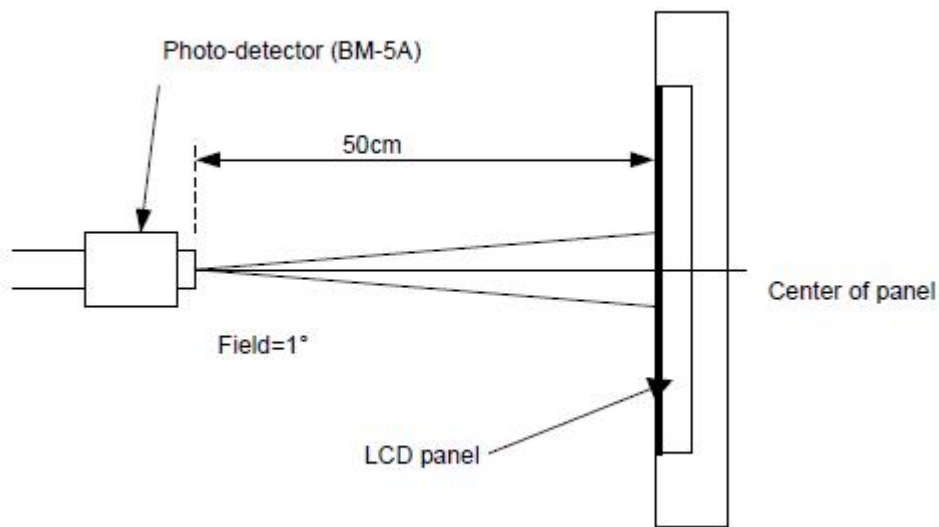
CR =

Luminance with all pixels black

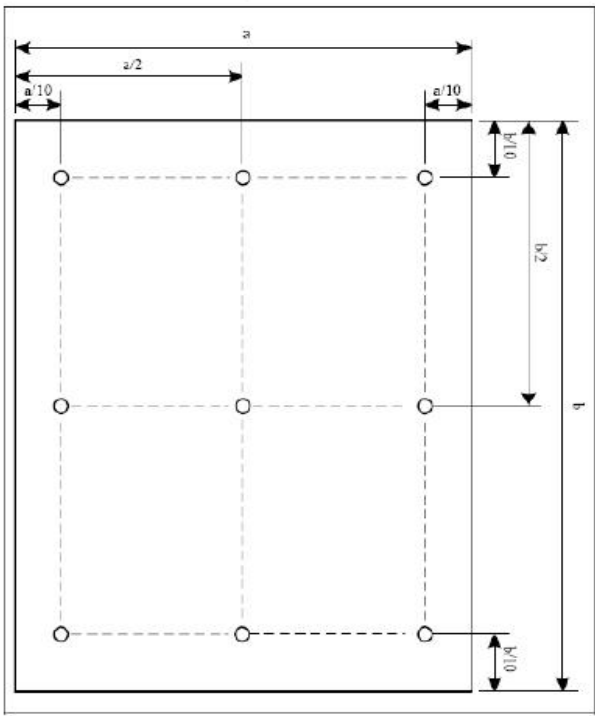
Note (3): Response Time



Note (4): Definition of optical measurement setup



NOTE (6): Luminance Uniformity of these 9 points is defined as below:



Uniformity = $\frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$

Luminance = $\frac{\text{Total Luminance of 9 points}}{9}$

5. AMOLED Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit	Note
I/O Voltage	VDDIO	--	6.6	V	Note1
Operation Voltage	VCI	--	6.6	V	
EL Driving Voltage	ELVDD	4.6	--	V	
EL Driving Voltage	ELVSS	-3	--	V	
Operating temperature	T _{OP}	-40	+85	°C	
Storage temperature	T _{ST}	-55	+125	°C	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Test Condition: Temp=25±2℃

Symbol	Min.	Typ.	Max.	Unit	Note
VCI	2.7	3.0	3.6	V	--
VDDIO	1.62	1.8	1.98	V	--
ELVDD	4.6	4.6	4.6	V	--
ELVSS	-3	-2	-1.4	V	--
AVDD	6.8	6.8	7.8		

1. The value is just the reference value. The customer can optimize the setting value by the different D-IC.
RM69700, Ramless.

6. AC Characteristics

6.1 Serial Interface Characteristics

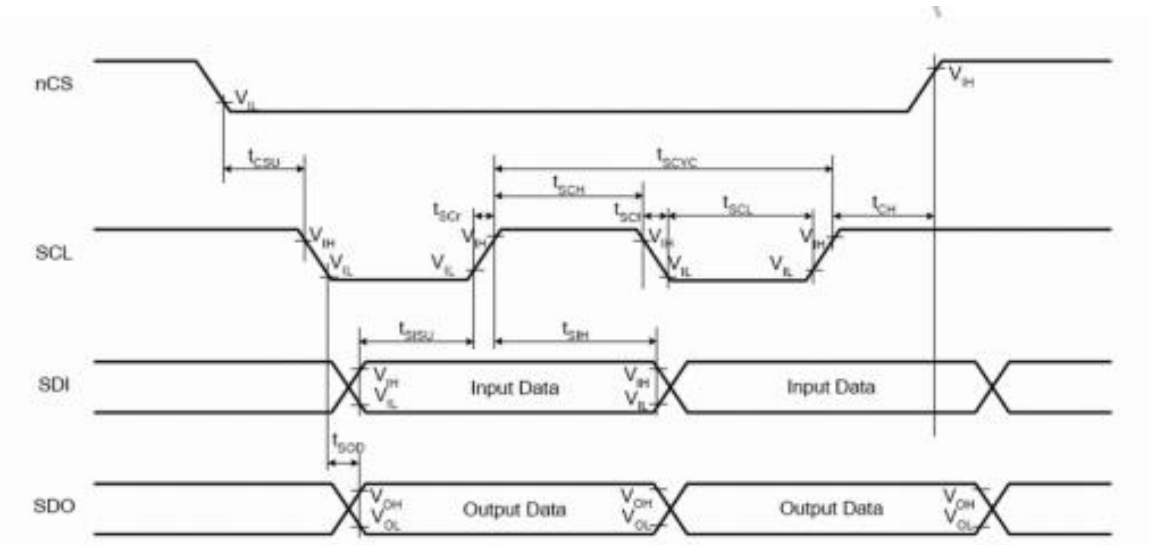


Figure 7.1

Table 7.1

Signal	Symbol	Parameter	MIN	MAX	Unit
SCL	T _{SCYC}	Clock cycle (Write)	100	-	ns
	T _{SCYC}	Clock cycle (Read)	300	-	ns
	T _{SCH}	Clock "H" pulse width (Write)	40	-	ns
	T _{SCH}	Clock "H" pulse width (Read)	140	-	ns
	T _{SCL}	Clock "L" pulse width (Write)	40	-	ns
	T _{SCL}	Clock "L" pulse width (Read)	140	-	ns
	T _{SCr}	Clock rise time	-	5	ns
	T _{SCf}	Clock fall time	-	5	ns
nCS	T _{CSU}	Chip select setup time	20	-	ns
	T _{CH}	Chip select hold time	50	-	ns
SDI	T _{SISU}	Data input setup time	20	-	ns
	T _{SIH}	Data input hold time	20	-	ns
SDO	T _{SOD}	Data output setup time	-	120	ns
	T _{SOH}	Data output hold time	5	-	ns

Notes:

- 1.Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.
- 2.Ta = -40°C to 85°C, VDDI=1.62V to 1.98V, VCI=2.5V to 3.6V, GND=0V

6.2 RGB Interface Characteristics

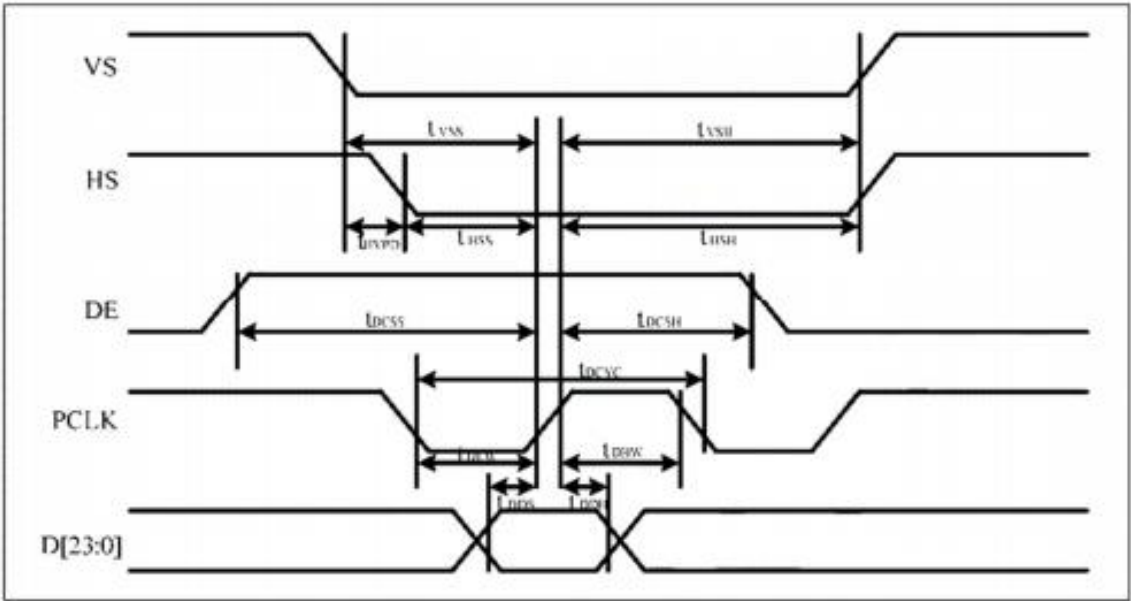


Figure 7.3

Table 7.3

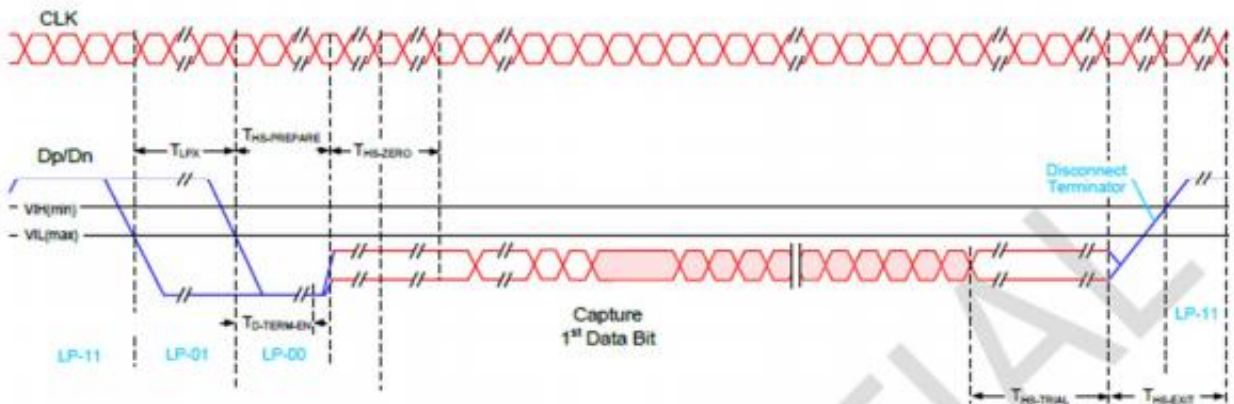
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit
PCLK	t_{PCLK}	PCLK cycle time	15	-	-	ns
	t_{PLW}	PCLK low pulse width	7	-	-	ns
	t_{PHW}	PCLK high pulse width	7	-	-	ns
VS	t_{VSS}	VS setup time	3	-	-	ns
	t_{VSH}	VS hold time	3	-	-	ns
HS	t_{HSS}	HS setup time	3	-	-	ns
	t_{HSH}	HS hold time	3	-	-	ns
	t_{HVPO}	HS to VS falling edge	400	-	-	ns
DE	t_{DCSS}	DE setup time	3	-	-	ns
	t_{DCSH}	DE hold time	3	-	-	ns
D[23:0]	t_{DDS}	Data setup time	3	-	-	ns
	t_{DDH}	Data hold time	3	-	-	ns

Notes:

- Logic high and low levels are specified as 20% and 80% of IOVCC for input signals.
- Ta=-40 to 85°C, IOVCC=1.62V to 1.98V, VCI=2.5V to 3.6V, GND=0V.

6.3 DSI Timing Characteristics

■ HS Data Transmission Burst



■ HS clock transmission

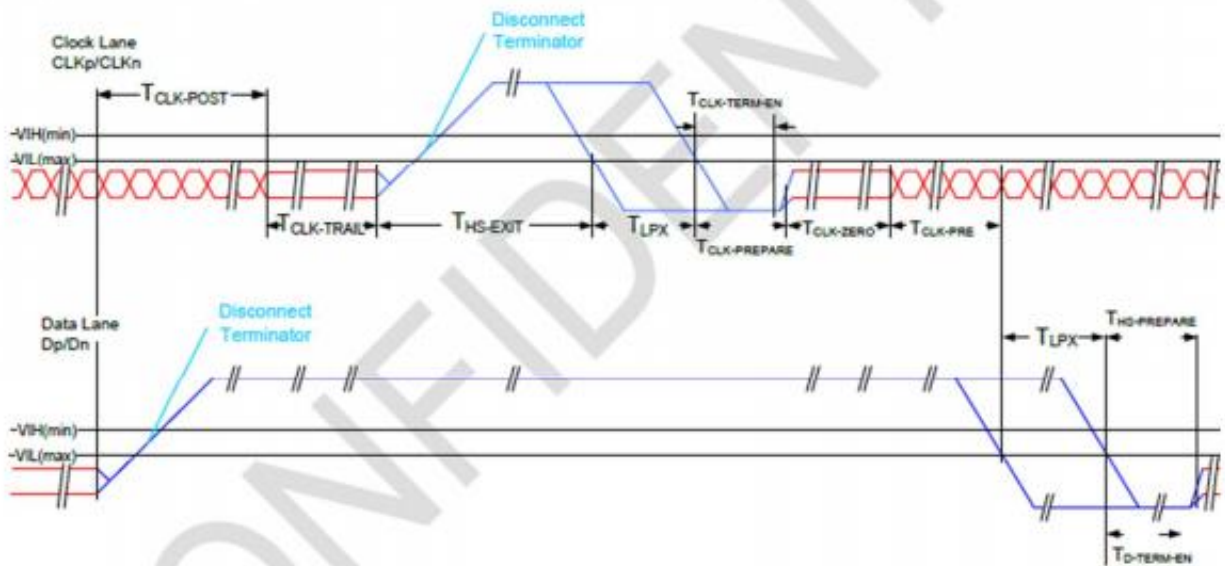


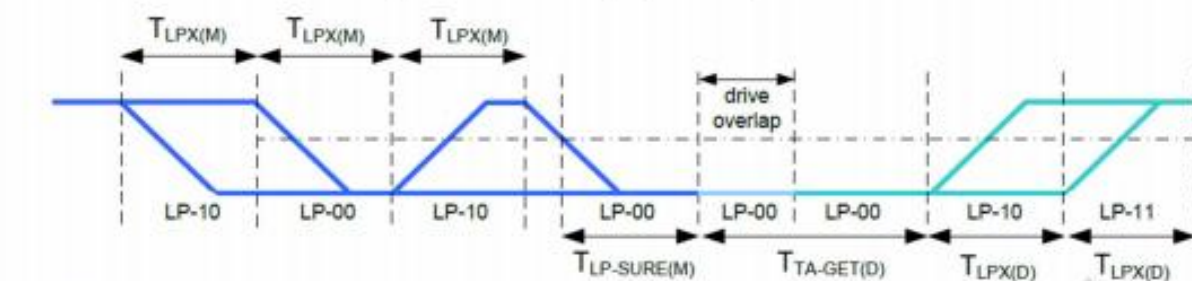
Figure 7.4

Table 7.4 Time parameter

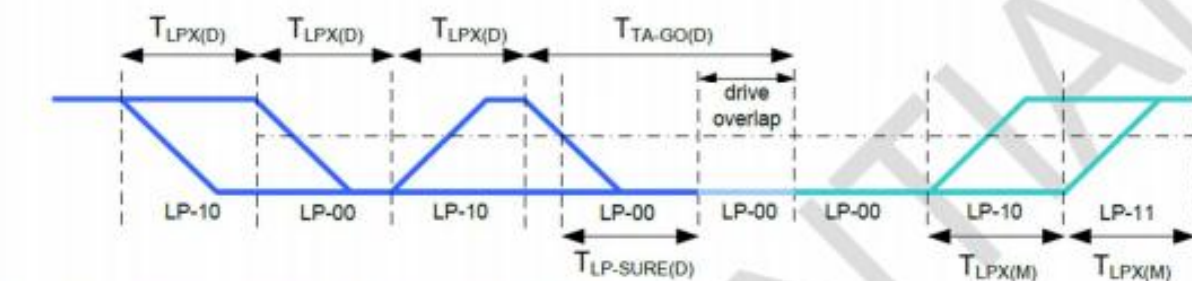
Parameter	Description	MIN	MAX	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRIAL}$ to the beginning of $T_{CLK-TRAIL}$.	$60ns+52 \times UI$		ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60		ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300		ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, Starting from the time point when	Time for Dn to reach $V_{TERM-EN}$	38	ns

	Dn crosses $V_{IL, MAX}$.			
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8		UI
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300		ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL, MAX}$.	Time for Dn to reach $V_{TERM-EN}$	$35ns + 4 \times UI$	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	$40ns + 4 \times UI$	$85ns + 6 \times UI$	ns
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145ns + 10 \times UI$		ns
$T_{HS-TRIAL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	$60ns + 4 \times UI$		ns

■ Bus Turnaround Procedure (From MPU to display module)



Bus turnaround (BAT) timing



Bus turnaround (BAT) from display module to MPU timing

Figure 7.5

Table 7.5

■ Timing Specifications for Low Power Transmission:

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2 \cdot T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5 \cdot T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4 \cdot T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2 \cdot T_{LPX(D)}$	ns	2

Notes:

1. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

6.4 Reset Timing

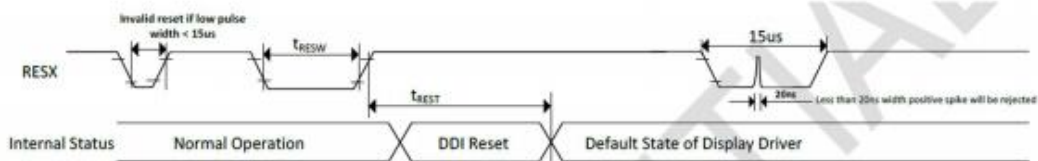


Figure 7.6

Table 7.6

Reset timing @VDDI=1.62V to 1.98V, VSSA=DVSS=VSSI=0V, Ta=-40°C to 85°C

Symbol	Parameter	MIN	TYP	MAX	Note	Unit
t_{RESW}	Reset low pulse width	15	-	-	1. Shorter than 5 μ s, Reset rejected 2. Longer than 15 μ s, IC reset 3. Between 5 μ s and 15 μ s, It depends on voltage and temperature condition.	μ s
t_{REST}	Reset complete time	-	-	10	When reset applied at sleep-in mode	ms
		-	-	120	When reset applied at sleep-out mode	ms

6.5 Touch Panel I2C Timing Characteristics

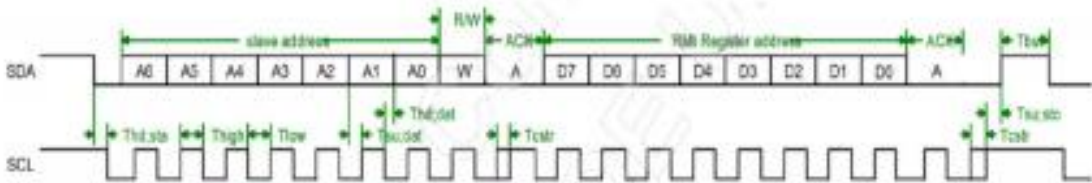


Figure 7.7

Table 7.7

Parameter	Symbol	Standard Mode			Fast Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
SCL clock frequency	f_{SCL}	-	-	100	-	-	400	kHz
Clock stretch time	t_{CSTR}	-	<25	-	-	<25	-	us
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD,STA}$	4.0	-	-	0.6	-	-	us
Low period of the SCL clock	t_{LOW}	4.7	-	-	1.3	-	-	us
High period of the SCL clock	t_{HIGH}	4.0	-	-	0.6	-	-	us
Setup time for repeated START condition	$t_{SU,STA}$	4.7	-	-	0.6	-	-	us
Data hold time	$t_{HD,DAT}$	0	-	-	0	-	-	us
Data out valid time	$t_{VAL,DAT}$	-	-	3.45	-	-	0.9	us
Data setup time	$t_{SU,DAT}$	250	-	-	100	-	-	ns
Rise time of SDA/SCL	t_R	-	-	1000	$20 + 0.1C_B$	-	300	ns
Fall time of SDA/SCL	t_F	-	-	300	$20 + 0.1C_B$	-	300	ns
Setup time for STOP condition	$t_{SU,STO}$	4.0	-	-	0.6	-	-	us
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	1.3	-	-	us
Capacitive load for each bus line	C_B	-	-	400	-	-	400	pF

6.6 Touch Panel Reset Timing Characteristics

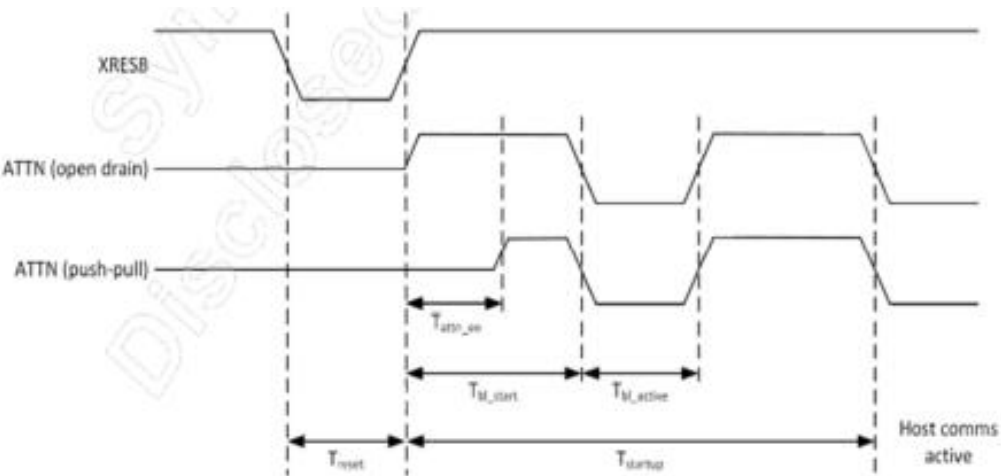


Figure 7.8

Table 7.8

Power supply	Min	Max	Unit
T_{atn_en}	5	21	ms
$T_{powerup}$	-	45	ms
$T_{startup}$	-	45	ms
T_{bl_start} (bootloader start)	-	30	ms
T_{bl_active} (bootloader active)	-	15	ms
T_{reset}	100	-	ns

7. Recommended Operating Sequence

7.1 Display Power on/off Sequence

Power Sequence and Generation

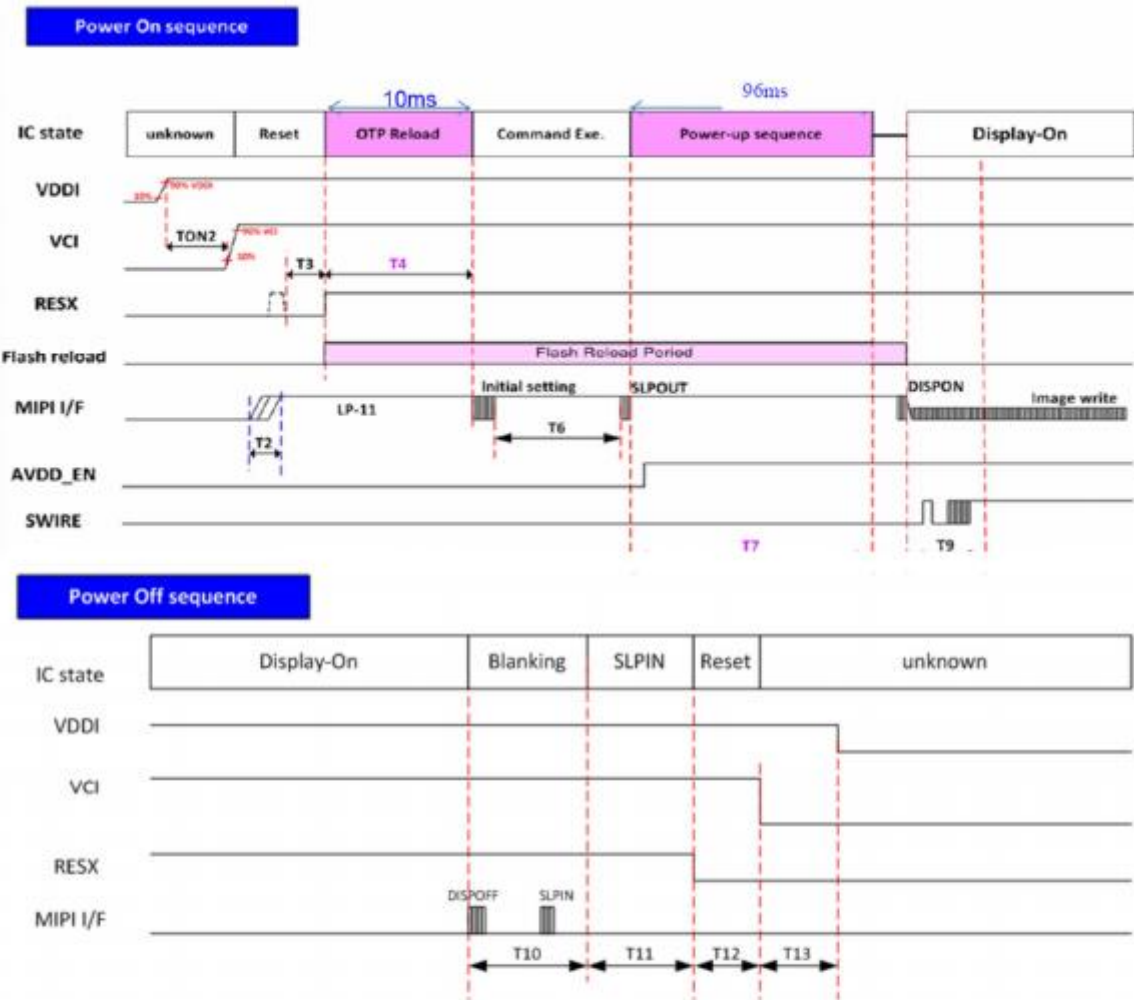


Figure 8.1

Timing Specification of Power On/Off Sequence

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
TON2	2	-	-	ms	
T2	1	-	-	ms	MIPI stabilization time
T3	1	-	-	ms	Effective hardware reset period
T4	10	-	-	ms	OTP reload time
T6	0	-	-	ms	Initial code input finish to SLPOUT command input
T7	-	96	-	ms	Normal power-up sequence
T9	2	-	-	VS	Display-On Blanking region
T10	2	-	-	VS	Display-Off blanking region
T11	1	-	-	VS	Blanking region
T12	1	-	-	ms	Effective hardware reset period
T13	2	-	-	ms	Power off period

7.2 Touch Panel Power on Sequence

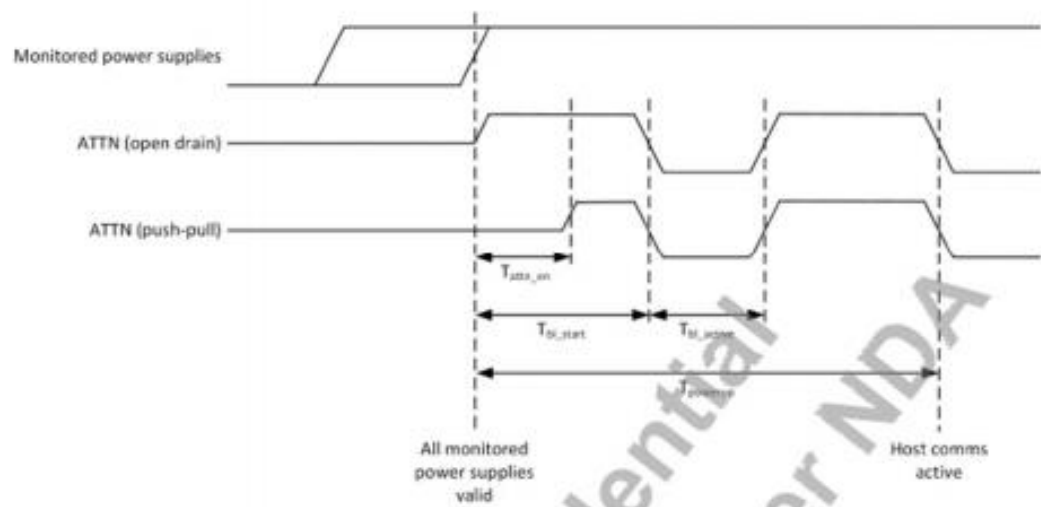


Figure 8.2

Table 8.1

Power supply	Min	Max	Unit
T_{attn_en}	5	21	ms
$T_{powerup}$	-	45	ms
$T_{startup}$	-	45	ms
T_{bl_start} (bootloader start)	-	30	ms
T_{bl_active} (bootloader active)	-	15	ms
T_{reset}	100	-	ns

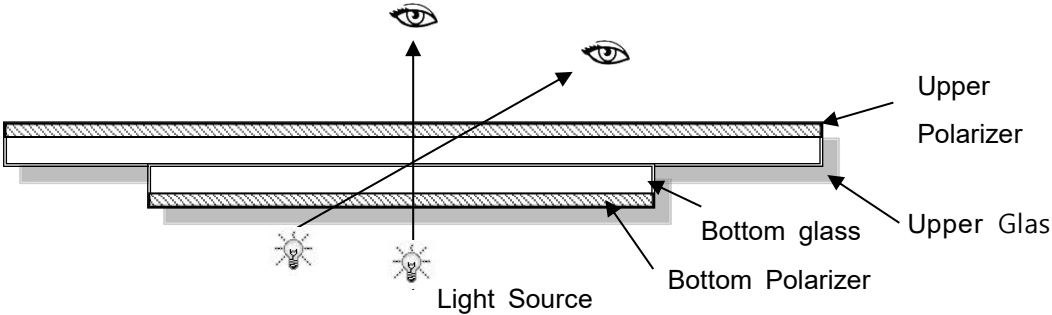
8. AMOLED Module Out-Going Quality Level

8.1 VISUAL & FUNCTION INSPECTION STANDARD

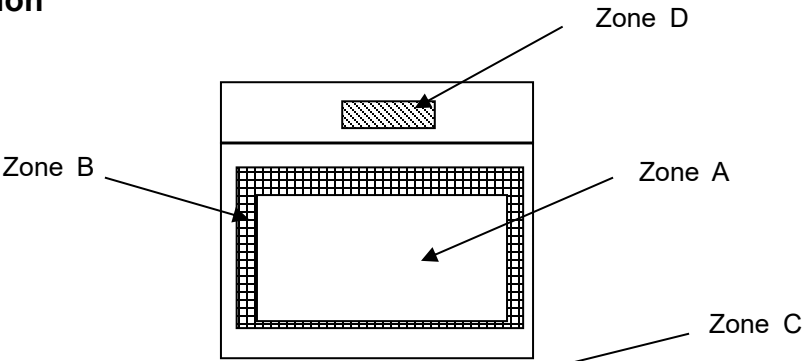
8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

- Temperature : 25±5°C
- Humidity : 65%±10%RH
- Viewing Angle : Normal viewing Angle.
- Illumination: Single fluorescent lamp (300 to 700Lux)
- Viewing distance:30-50cm



8.1.2 Definition



- Zone A : Effective Viewing Area(Character or Digit can be seen)
- Zone B : Viewing Area except Zone A
- Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)
- Zone D : IC Bonding Area

Note:
As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

8.1.3 Sampling Plan

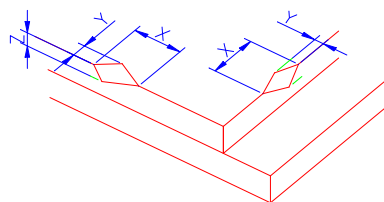
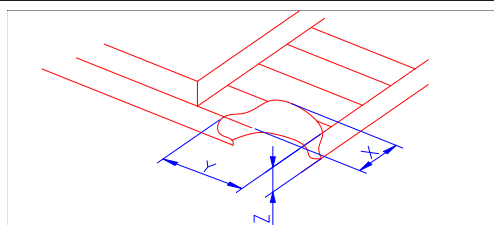
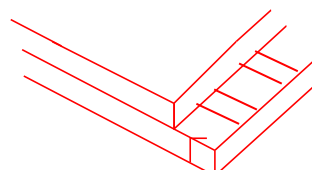
According to GB/T 2828-2003 ; , normal inspection, Class II
AQL:

Major defect	Minor defect
0.65	1.5

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc	Major
2	Missing	Missing components and etc	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc	
7	AMOLED/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which AMOLED panel is displaying under black pattern.
b) Dim dot: Dots appear dark and unchanged in size in which AMOLED panel is displaying under pure red, green, blue picture.

8.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 AMOLED Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of IT O, T: Height of AM OELD	(1) The edge of AMO LED broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)AMOLED corner broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) AMOLED crack	 Crack Not allowed							

Spot defect

2.0

Φ=(X+Y)/2

① light dot (black/white spot , pinhole, stain , etc.)

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.10	Ignore	Ignore	
0.10<Φ≤0.25	4(distance ≥ 10mm)		
0.25<Φ≤0.35	3		
Φ>0.4	0		

② Dim spot (light leakage、dent、dark spot , etc)

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore	Ignore	
0.10<Φ≤0.25	4(distance ≥ 10mm)		
0.25<Φ≤0.35	3		
Φ>0.4	0		

③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.5	3(distance ≥ 10mm)		
Φ>0.5	1		

④Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.10<Φ≤0.25	2(distance ≥ 10mm)		
0.25<Φ≤0.35	1		
Φ>0.4	0		

3.0	AMOLED Pixel defect	Pixel bad points <table border="1" data-bbox="539 309 1500 1057"> <thead> <tr> <th data-bbox="539 309 730 360">Item</th><th data-bbox="730 309 1244 360">Zone A</th><th data-bbox="1244 309 1500 360">Acceptable Qt</th></tr> </thead> <tbody> <tr> <td data-bbox="539 360 730 521" rowspan="3">Bright dot</td><td data-bbox="730 360 1244 416">Random</td><td data-bbox="1244 360 1500 416">$N \leq 2$</td></tr> <tr> <td data-bbox="730 416 1244 472">2 dots adjacent</td><td data-bbox="1244 416 1500 472">$N \leq 0$</td></tr> <tr> <td data-bbox="730 472 1244 521">3 dots adjacent</td><td data-bbox="1244 472 1500 521">$N \leq 0$</td></tr> <tr> <td data-bbox="539 521 730 689" rowspan="3">Dark dot</td><td data-bbox="730 521 1244 577">Random</td><td data-bbox="1244 521 1500 577">$N \leq 3$</td></tr> <tr> <td data-bbox="730 577 1244 633">2 dots adjacent</td><td data-bbox="1244 577 1500 633">$N \leq 0$</td></tr> <tr> <td data-bbox="730 633 1244 689">3 dots adjacent</td><td data-bbox="1244 633 1500 689">$N \leq 0$</td></tr> <tr> <td data-bbox="539 689 730 1003">Distance</td><td data-bbox="730 689 1244 1003"> 1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot. </td><td data-bbox="1244 689 1500 1003">5mm</td></tr> <tr> <td colspan="2" data-bbox="539 1003 1244 1057">Total bright and dark dot</td><td data-bbox="1244 1003 1500 1057">$N \leq 4$</td></tr> </tbody> </table> Note: A) Bright dot: Dots appear bright and unchanged in size in which AMOLED panel is displaying under black pattern. B) Dark dot: Dots appear dark and unchanged in size in which AMOLED panel is displaying under pure red, green, blue picture. C) 2 dot adjacent = 1 pair = 2 dots Picture: 2 dot adjacent 2 dot adjacent 2 dot adjacent (vertical) 2 dot adjacent (slant)	Item	Zone A	Acceptable Qt	Bright dot	Random	$N \leq 2$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Dark dot	Random	$N \leq 3$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm	Total bright and dark dot		$N \leq 4$
Item	Zone A	Acceptable Qt																							
Bright dot	Random	$N \leq 2$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Dark dot	Random	$N \leq 3$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm																							
Total bright and dark dot		$N \leq 4$																							

4.0	Line defect (AMOLED /Polarizer backlight black/white line, scratch, stain)  W: width, L : length N : Count					
		Width(mm)	Length(m)	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.05$	Ignore	Ignore		Ignore
		$0.05 < W \leq 0.06$	$L \leq 5.0$	$N \leq 3$		
		$0.07 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$		
$W > 0.08$	Define as spot defect					
5.0	Electronic Components SMT.	Not allow missing parts , solderless connection , cold solder joint , mismatch , The positive and negative polarity opposite				
6.0	Display color& Brightness.	1. Color : Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness : Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.				

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

9. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	85°C,96H	IEC60068-2-2,GB2423.2
Low Temperature Operating	-40°C, 96HR	IEC60068-2-1 GB2423.1
High Temperature Storage	125°C, 96HR	IEC60068-2-2 GB2423.2
Low Temperature Storage	-550°C, 96HR	IEC60068-2-1 GB2423.1
High Temperature & High	+60°C, 90% RH ,96 hours.	IEC60068-2-78 GB/T2423.3
Thermal Shock (Non-operation)	-40°C,30 min ↔ 80°C,30 min, Change time:5min 20CYC.	Start with cold temperature, End with high temperature, IEC60068-2-14,GB2423.22

Note: Product reliability items in the form of GK are used as reference items. The test results shall refer to the results of the reliability test of Visionox standards.

10. Cautions and Handling Precautions

10.1 Handling Precautions:

- (1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from height..
 - (2) Do not press down the screen or the adjoining areas too hard because the color tone may be shifted.
 - (3) The polarizer covering the display surface of the AMOLED module is soft and easily scratched. Handle this polarizer carefully.
 - (4) If the display surface is contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is still not completely clear, moisten the cloth with ethyl alcohol.
 - (5) Solvents may damage the polarizer. Do not use water, ketone or aromatic solvents except ethyl alcohol.
- Do not attempt to disassemble the AMOLED Module.
- (6) If the logic circuit power is off, do not apply the input signals.
 - (7) To prevent destruction from static electricity, be careful to maintain an optimum working environment.
 - (8) Be sure to make yourself in contact with the ground when handling with the AMOLED Modules.
 - (9) Tools required for assembly, such as soldering irons, must be properly ground.
 - (10) To reduce the generation of static electricity, do not conduct assembly or other work under dry conditions.
 - (11) To protect the display surface, the AMOLED Module is coated with a film. Be careful when peeling off this protective film, because static electricity may generate.

10.2 Storage Precautions.

- (1) When storing the AMOLED modules, be sure that they are not directly exposed to the sunlight or the light of fluorescent lamps.
- (2) The AMOLED modules should be stored under the storage temperature range. If the AMOLED modules will be stored for a long time, the recommended condition is: Temperature: 0℃~40℃ Relatively humidity: ≤80%
- (3) The AMOLED modules should be stored in the room without acid, alkali or harmful gas.

10.3 Transportation Precautions:

- (1) The AMOLED modules should not be suffered from falling and violent shocking during transportation. Besides, excessive press, water, damp and sunshine, should be avoided.

11. Packing

----TBD-----